IN THE CLAIMS

Please amend the claims as follows:

1.-3. (Canceled)

4.   (Currently Amended) A method comprising:

delaying a first clock signal to produce a delayed clock signal;

generating the first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal;

measuring time intervals between phases of the first clock signal, wherein measuring the time intervals comprises determining a first duty cycle skew of the first clock signal by adjusting a time delay between the first clock signal and the delayed clock signal, and comparing the first clock signal and the delayed clock signal The method of claim 3, wherein determining the first duty cycle skew comprises[[:]] adjusting the time delay to a first value, which indicates a first time delay when a first delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock signal[[;]], adjusting the time delay to a second value, which indicates a second time delay when a second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first clock signal[[;]], and determining the first duty cycle skew based on the first time delay and the second time delay; and

adjusting the delayed clock signal based on the time intervals.

5.   (Currently Amended) A method comprising:

delaying a first clock signal to produce a delayed clock signal;

generating the first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal;

measuring time intervals between phases of the first clock signal, wherein measuring the

time intervals comprises determining a first duty cycle skew of the first clock signal by adjusting

a time delay between the first clock signal and the delayed clock signal, and comparing the first

clock signal and the delayed clock signal; and

adjusting the delayed clock signal based on the time intervals ~~The method of claim 3~~,

wherein adjusting the delayed clock signal comprises[[:]] producing a third clock signal with a

second duty cycle skew, wherein the second duty cycle skew is less than the first duty cycle

skew by a time difference that is based on the first duty cycle skew.

6.   (Original) A method comprising:

generating a first clock signal from an input clock signal, wherein the first clock signal

includes first pulses, which correspond to leading edges of the input clock signal, and second

pulses, which correspond to falling edges of the input clock signal;

delaying the first clock signal by a time delay to produce a delayed clock signal having

first delayed pulses and second delayed pulses;

determining a first duty cycle skew of the first clock signal by adjusting the time delay

and comparing the first clock signal and the delayed clock signal; and

producing a third clock signal with a second duty cycle skew, wherein the second duty

cycle skew is less than the first duty cycle skew by a time difference that is based on the first

duty cycle skew.

7.   (Original) The method of claim 6, wherein determining the first duty cycle skew

comprises:

adjusting the time delay to a first value, which indicates a first time delay when a first

delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock

signal;

adjusting the time delay to a second value, which indicates a second time delay when a

second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first

clock signal; and

determining the first duty cycle skew based on the first time delay and the second time

delay.

8.   (Original) The method of claim 6, wherein producing the third clock signal comprises:

        calculating a skew adjustment value as approximately one half of a difference between

the first time delay and the second time delay; and

        applying the skew adjustment value to a clock signal to produce the third clock signal.

9.-11. (Canceled)

12.   (Original) An apparatus comprising:

        a clock generator, which functions to generate a first clock signal from an input clock

signal, wherein the first clock signal includes first pulses, which correspond to leading edges of

the input clock signal, and second pulses, which correspond to falling edges of the input clock

signal;

        a delay element, operatively coupled to the clock generator, which functions to delay the

first clock signal by a time delay to produce a delayed clock signal having first delayed pulses

and second delayed pulses; and

        a first circuit, operatively coupled to the delay element, which functions to determine a

first duty cycle skew of the first clock signal by adjusting the time delay and comparing the first

clock signal and the delayed clock signal, and which further functions to provide control

information for producing a third clock signal with a second duty cycle skew, wherein the second

duty cycle skew is less than the first duty cycle skew by a time difference that is based on the

first duty cycle skew.

13.   (Original) The apparatus of claim 12, wherein the first circuit determines the first duty

cycle skew by:

        adjusting the time delay to a first value, which indicates a first time delay when a first

delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock

signal;

        adjusting the time delay to a second value, which indicates a second time delay when a

second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first

clock signal; and

determining the first duty cycle skew based on the first time delay and the second time delay.

14.   (Original) The apparatus of claim 12, wherein the first circuit provides the control information by:

calculating a skew adjustment value as approximately one half of a difference between the first time delay and the second time delay; and

applying the skew adjustment value to a clock signal to produce the third clock signal.

15.-17. (Canceled)

18.   (Original) A microprocessor comprising:

a clock generator, which functions to generate a first clock signal from an input clock signal, wherein the first clock signal includes first pulses, which correspond to leading edges of the input clock signal, and second pulses, which correspond to falling edges of the input clock signal;

a delay element, operatively coupled to the clock generator, which functions to delay the first clock signal by a time delay to produce a delayed clock signal having first delayed pulses and second delayed pulses; and

a first circuit, operatively coupled to the delay element, which functions to determine a first duty cycle skew of the first clock signal by adjusting the time delay and comparing the first clock signal and the delayed clock signal, and which further functions to provide control information for producing a third clock signal with a second duty cycle skew, wherein the second duty cycle skew is less than the first duty cycle skew by a time difference that is based on the first duty cycle skew.

19.   (Original) The microprocessor of claim 18, wherein the first circuit determines the first duty cycle skew by:

adjusting the time delay to a first value, which indicates a first time delay when a first

delayed pulse of the delayed clock signal occurs in proximity to a second pulse of the first clock

signal;

adjusting the time delay to a second value, which indicates a second time delay when a

second delayed pulse of the delayed clock signal occurs in proximity to a first pulse of the first

clock signal; and

determining the first duty cycle skew based on the first time delay and the second time

delay.

20.   (Original) The microprocessor of claim 18, wherein the first circuit provides the control

information by:

calculating a skew adjustment value as approximately one half of a difference between

the first time delay and the second time delay; and

applying the skew adjustment value to a clock signal to produce the third clock signal.

21.   (New) An apparatus comprising:

a delay element to delay a first clock signal to produce a delayed clock signal;

a clock generator to generate the first clock signal from an input clock signal, wherein the

first clock signal includes first pulses, which correspond to leading edges of the input clock

signal, and second pulses, which correspond to falling edges of the input clock signal;

a circuit to measure time intervals between phases of the first clock signal by determining

a first duty cycle skew of the first clock signal by adjusting a time delay between the first clock

signal and the delayed clock signal, and by comparing the first clock signal and the delayed

clock signal, wherein determining the first duty cycle skew comprises adjusting the time delay to

a first value, which indicates a first time delay when a first delayed pulse of the delayed clock

signal occurs in proximity to a second pulse of the first clock signal, adjusting the time delay to a

second value, which indicates a second time delay when a second delayed pulse of the delayed

clock signal occurs in proximity to a first pulse of the first clock signal, and determining the first

duty cycle skew based on the first time delay and the second time delay, and wherein the circuit

is to adjust the delayed clock signal based on the time intervals.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111
Serial Number: 10/718,282
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Title: A DEVICE AND METHOD TO DETECT AND CORRECT FOR CLOCK DUTY CYCLE SKEW IN A PROCESSOR
Assignee: Intel Corporation

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22.   (New) The apparatus of claim 21, wherein the first circuit is to provide control information for producing a third clock signal with a second duty cycle skew, wherein the second duty cycle skew is less than the first duty cycle skew by a time difference that is based on the first duty cycle skew.